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AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listings, of claims in the application.

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1. (ORIGINAL) An integrated circuit including logic for testing internal operation of the integrated circuit, the integrated circuit comprising:

a plurality of internal functional blocks coupled by a plurality of internal buses, wherein the plurality of internal functional blocks and the plurality of internal buses are comprised in the integrated circuit;

a set of test control input pins comprised on the integrated circuit;

a set of test output pins comprised on the integrated circuit; and

selection logic comprised in the integrated circuit, wherein the selection logic comprises:

a plurality of inputs coupled to two or more of the plurality of internal buses;

at least one select input coupled to receive select signals from the set of test control input pins; and

an output coupled to the set of test output pins;

wherein the selection logic is operable to select internal bus signals from one of the two or more internal buses based on the select signals from the test control input pins, wherein the selection logic is configured to output the selected internal bus signals to the set of test output pins.

2. (ORIGINAL) The integrated circuit of claim 1,

wherein the selection logic further comprises a plurality of inputs coupled to two or more of the plurality of internal functional blocks;

wherein the selection logic is operable to select functional block signals from one of the two or more internal functional blocks based on the select signals from the test control input pins, wherein the selection logic is configured to output the selected functional block signals to the set of test output pins.

3. (ORIGINAL) The integrated circuit of claim 1, further comprising interface logic coupled between at least one of the plurality of inputs of the selection logic and at least one of the plurality of internal buses, wherein the interface logic is configured to buffer data from the at least one internal bus before the data is output to the set of test output pins.

4. (ORIGINAL) The integrated circuit of claim 1,

wherein a first internal functional block is operable to provide first internal functional block output signals, wherein the first internal functional block output signals are operable to be selectively coupled to the output of the selection logic.

5. (ORIGINAL) The integrated circuit of claim 1, wherein each internal bus comprises a plurality of parallel data lines operating at a single high frequency.

6. (ORIGINAL) The integrated circuit of claim 1, wherein data from a selected internal bus is output in parallel via the set of test output pins at a frequency equal to the operating frequency of the selected internal bus.

7. (ORIGINAL) The integrated circuit of claim 1, wherein the integrated circuit further comprises boundary scan logic and pins.

8. (ORIGINAL) The integrated circuit of claim 1, wherein the selection logic is implemented using small transistor sizes that are limited to switching at a significantly slower clock frequencies than the functional blocks.

9. (ORIGINAL) The integrated circuit of claim 1, wherein the selection logic comprises at least one multiplexer.

10. (ORIGINAL) The integrated circuit of claim 1, wherein the integrated circuit is an application specific integrated circuit.

11. (ORIGINAL) The integrated circuit of claim 1, wherein the selection logic is configured to select and output the selected internal bus signals to the set of test output pins in real time.

12. (ORIGINAL) An integrated circuit including logic for testing internal operation of the integrated circuit, the integrated circuit comprising:

a plurality of internal functional blocks coupled by a plurality of internal buses, wherein the plurality of internal functional blocks and the plurality of internal buses are comprised in the integrated circuit;

at least one test control input pin comprised on the integrated circuit;

a set of test output pins comprised on the integrated circuit; and

selection logic comprised in the integrated circuit, wherein the selection logic comprises:

a plurality of inputs coupled to two or more of the plurality of internal buses;

at least one select input coupled to receive at least one select signal from the at least one test control input pin; and

an output coupled to the set of test output pins;

wherein the selection logic is operable to select internal bus signals from one of the two or more internal buses based on the at least one select signal from the at least one test control input pin, wherein the selection logic is configured to output the selected internal bus signals to the set of test output pins.

13. (ORIGINAL) An integrated circuit including logic for testing internal operation of the integrated circuit, the integrated circuit comprising:

a plurality of internal functional blocks coupled by a plurality of internal buses, wherein the plurality of internal functional blocks and the plurality of internal buses are comprised in the integrated circuit;

at least one test control input pin comprised on the integrated circuit;

a set of test output pins comprised on the integrated circuit; and

selection logic comprised in the integrated circuit, wherein the selection logic comprises:

a plurality of inputs coupled to two or more of the plurality of internal functional blocks;

at least one select input coupled to receive at least one select signal from the at least one test control input pin; and

an output coupled to the set of test output pins;

wherein the selection logic is operable to select internal functional block signals from one of the two or more internal functional blocks based on the at least one select signal from the at least one test control input pin, wherein the selection logic is configured to output the selected internal functional block signals to the set of test output pins.

14. (ORIGINAL) A system for testing an integrated circuit having two or more internal functional blocks coupled by two or more internal buses, the system comprising:

a set of test control inputs;

a set of parallel test outputs;

selection logic configured to select one of the two or more internal buses in response to one or more control signals from the test control inputs, wherein the selection logic is configured to output signals from the selected internal bus to the parallel test outputs.

15. (ORIGINAL) The system of claim 14,

wherein the selection logic is configured to select one of the two or more internal functional blocks in response to one or more control signals from the test control inputs, wherein the selection logic is configured to output signals from the selected internal functional block to the parallel test outputs.

16. (ORIGINAL) An application specific integrated circuit, comprising:

a plurality of functional units;

a plurality of internal buses connecting the functional units;

one or more control pins;

a plurality of test pins; and

multiplexing logic coupled to at least a subset of the plurality of internal buses and the test pins, wherein the multiplexing logic is configured to select one of the plurality of internal buses in response to one or more control signals conveyed to the multiplexing logic from the

control pins, wherein the multiplexing logic is configured to output signals from the selected internal bus to the test pins in real-time.

17. (ORIGINAL) The application specific integrated circuit of claim 16,

wherein the multiplexing logic is configured to select one of the plurality of functional units in response to the one or more control signals conveyed to the multiplexing logic from the control pins, wherein the multiplexing logic is configured to output signals from the selected functional unit to the test pins in real-time.

18. (ORIGINAL) The application specific integrated circuit of claim 17, further comprising:

interface logic configured to interface between the selected internal bus operating at a first clock rate, and the output pins operating at a second clock rate.

19. (ORIGINAL) The application specific integrated circuit of claim 17, wherein the test pins are configurable for non-test use by a control signal delivered to the selection logic via the one or more control pins.

20. (ORIGINAL) The application specific integrated circuit of claim 16, wherein one of the internal buses is an output bus, and wherein the test pins also operate as output pins.

21. (CANCELLED) A computer program for testing integrated circuits, wherein the computer program is embodied on a computer-readable medium and comprises instructions executable to:

receive user-specified information regarding which of a plurality of internal buses on an integrated circuit are to be made available for testing purposes;

calculate a size of selection logic and number of control signals required to selectively convey the information on the internal buses to a set of test pins; and

provide the results of the calculations to an automated place-and-route routine that determines the physical layout of the integrated circuit.

22. (CANCELLED) The computer program of claim 21, wherein the integrated circuit is an application specific integrated circuit (ASIC).

23. (CANCELLED) A method for testing an integrated circuit, the method comprising:

conveying a control signal to one or more test control pins on the integrated circuit;

selecting one of a plurality of internal buses for output to a set of parallel output pins on the integrated circuit in response to the control signal.

24. (CANCELLED) The method of claim 23, further comprising recording the signals output on the parallel output pins, wherein the signals output vary in real time relative to the selected internal bus.

25. (CANCELLED) The method of claim 23, further comprising periodically changing the control signal to cause the selection logic to change which of the internal buses' signals are output to the parallel output pins.